Suppression of Parasitic Substrate Modes in Flip-Chip Packaged Coplanar W-Band Amplifier MMICs

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***Abstract* – In this work, we describe the impact of different mounting configurations for flip-chip assemblies of W-band millimeter-wave integrated circuits (MMICs). Coplanar 94 GHz amplifiers with high gain have been flip-chip mounted on both, semi-insulating (s.i.) GaAs and n-type doped silicon (n-Si) carriers. The influence of carrier thickness and conductivity on the isolation between the input and output port was investigated to minimize the power leakage into parasitic modes in the flip-chip substrate. The use of lossy n-Si substrates resulted in a significant reduction of feed back and crosstalk effects, and thus an unconditional stable operation of the flip-chip packaged W-band amplifier MMICs was achieved.**

I. Introduction

Recent developments lead to an increasing interest in monolithic millimeter-wave integrated circuits for the realization of wireless communication and radar systems as well as for sensor applications [1,2]. At W-band frequencies these systems offer high resolution, large bandwidth and small size when using MMICs. The two major transmission line technologies for integrated circuits are the microstrip line and the coplanar waveguide. The microstrip technology shows low line loss and good thermal heat dissipation, due to the use of thin substrates [3]. The advantage of coplanar circuits, as demonstrated in this work, is that they allow very compact designs, due to the reduced crosstalk of adjacent lines. Additionally, coplanar technology is well suited for flip-chip mounting because of the one-sided level of metallization. Apart from the technical feasibility of high frequency circuits and subsystems, the packaging technology is becoming a major task. Flip-chip mounting allows for very short connections between the carrier substrate and the chip and can be applied for the packaging of millimeter-wave circuits up to W-band frequencies [4,5]. Further advantages of this interconnection technique are low transition losses and small mismatch. The implementation of thermal bumps, which are placed between the gatefingers of the transistors, results in lower device temperature and therefore higher reliability.

For increasing operation frequencies, the impact of power leakage into unwanted substrate modes, becomes ever more important. These modes propagate in both, the substrate of the mounted chip and the carrier substrate, and result in additional feed back and crosstalk, which directly effect circuit stability and performance [6,7].

In this work, we investigated the influence of different substrate parameters on the stability of flip-chip mounted 94 GHz high gain amplifiers [8]. In addition to semi-insulating GaAs flip-chip substrates, doped Si carriers with low resistivity were examined. The amplifier MMICs packaged on GaAs carriers showed a degradation of the circuit behavior. Mounting on lossy Si substrates improved the performance significantly. Thus, unconditional stable operation and a flat gain response was achieved with this technique, due to reduced feed back and crosstalk effects.

II. Amplifier Performance: On-Wafer and Single-Chip

On-wafer measured S-parameters of integrated 94 GHz amplifier circuits can already indicate the effects of unwanted substrate modes. At W-band frequencies, the power leakage into surface waves and parallel-plate modes becomes more and more significant and causes degradation of the circuit performance. Crosstalk and feed back effects result in strong ripples in the measured small-signal gain curve (Fig. 1) or even circuit failure. The instability is illustrated in Fig. 2 by a stability factor (µ-factor) lower 1. After dicing the amplifier chip, the effect of unwanted modes becomes ever more pronounced. Substrate resonances and multiple-mode interference, due to reflections of substrate modes on the finite substrate walls [9], decreased the isolation of the amplifier chip to values around 25 dB, as shown in Fig. 1. In order to reduce the influence of surface waves and to obtain a stable circuit operation, the single chip was thinned to 100 µm and a 2 mm thick quartz underfill was used for the measurement. This method increased the isolation to about 50 dB. Moreover, a flat gain curve and a µ-factor greater than 1 was

achieved. The quartz substrate suppressed the excitation of parallel-plate modes between the metalized chip surface and the metal chuck of the measurement system and thus prevents degradation of the circuit performance [10].

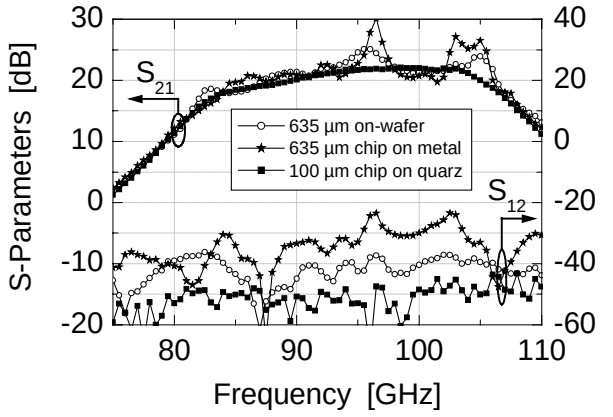

Fig. 1. Measured gain and isolation of a coplanar W-band amplifier circuit on-wafer and single-chip on two different carriers.

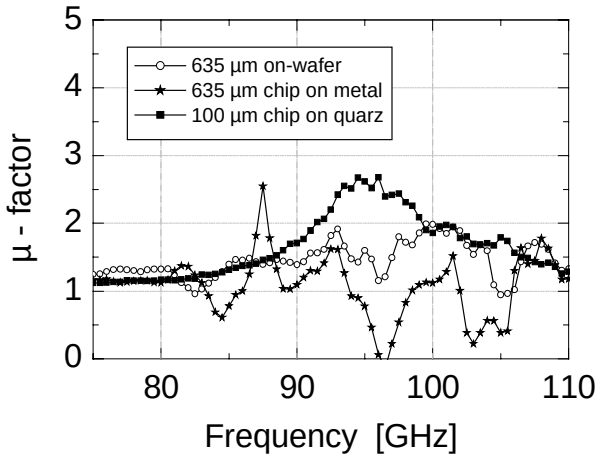

Fig. 2. Measured stability factor (µ-factor) of a coplanar W-band amplifier circuit on-wafer and single-chip on two different carriers.

III. Flip-Chip Packaging on GaAs Substrates

Flip-chip packaging of GaAs MMICs on GaAs substrates offers the advantage that both, the chip and the flip-chip substrate have the same thermal expansion coefficient. Thus, we investigated flip-chip packaging of thick and thin amplifier chips on GaAs substrates with different heights. To realize the flip-chip bumps, a 17 µm gold wire was formed by electrical flame-off and attached to the substrate with a thermosonic ball bonder. The diameter and the height of the realized gold bumps were about 60 µm. To mount the chips, a Carl Suess FC 150 flip-chip bonder applying a thermo-compression process was utilized. The measured small-signal gain (S_{21}) and isolation (S_{12}) of flip-chip packaged 94 GHz amplifier MMICs are shown in Fig. 3.

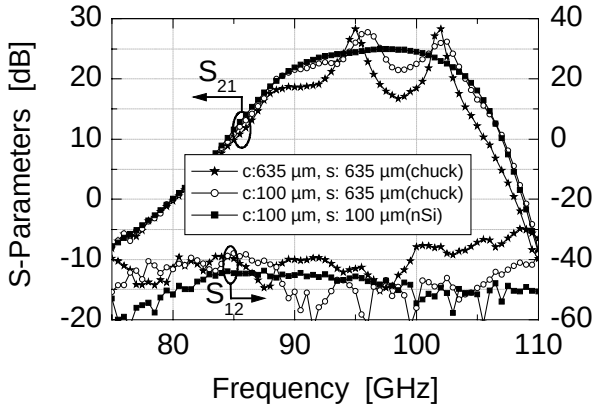

Fig. 3. Measured gain and isolation of flip-chip mounted W-band amplifier MMICs for different chip (c) and substrate (s) heights. The circuits were measured on a metal chuck and on a n-type doped Si (19 Ω·cm) wafer.

The 635 µm thick amplifier chip on the 635 µm thick GaAs flip-chip substrate had a minimum isolation of only 30 dB and large peaks in the gain characteristic. A µ-factor lower 1, as shown in Fig. 4, validates an unstable circuit behavior. The excitation of surface waves can be reduced by thinning the chip, as stated in section II. This was verified by the S-parameter measurements of a thin amplifier chip on a 635 µm flip-chip substrate, now showing a µ-factor greater than 1. However, the parasitic substrate modes excited in the thick flip-chip carrier caused significant ripples of the gain characteristic. The best results were obtained with a 100 µm chip mounted on a 100 µm thin GaAs flip-chip substrate. For this configuration, a flat gain curve and an unconditional stable amplifier behavior was achieved, using a lossy Si wafer as underfill for the measurements (Fig. 3 and Fig. 4).

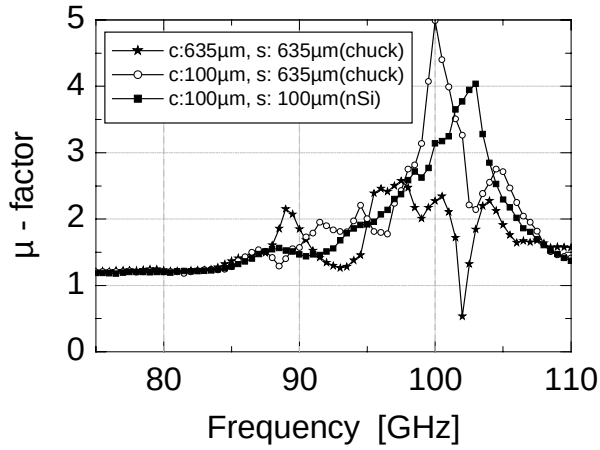

Fig. 4. Measured µ-factor of the flip-chip mounted W-band amplifier MMICs of Fig. 3.

IV. Flip-Chip Substrate Properties

As shown in III, the substrate properties are of prime importance for flip-chip packaging. The suppression of parasitic substrate modes is the major issue when choosing the suited substrate material, aside from factors like cost, thermal conductivity and the thermal expansion coefficient. Figure 5 shows the layout of a typical carrier substrate, which was used for flip-chip mounting. The planar transmission lines were realized as finite ground coplanar waveguides (FGCPW), in order to reduce the excitation of parallel-plate modes in the flip-chip substrate [11].

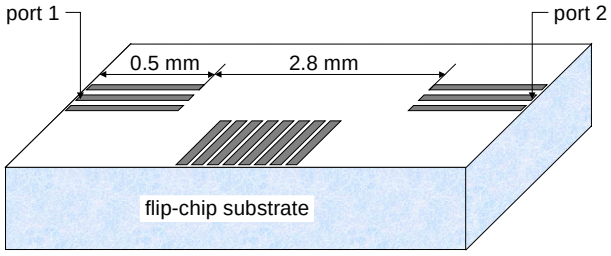

Fig. 5. Layout of a flip-chip substrate with finite ground coplanar waveguides (FGCPW) and bias lines.

The crosstalk between port 1 and port 2 was investigated with flip-chip substrates realized on both, s.i. GaAs and doped Si (19 Ω·cm). The isolation was measured for different substrate heights, as shown in Fig. 6. With the 635 µm GaAs substrate, a value of only 35 dB was achieved. By thinning the carrier down to 100 µm the isolation was improved to approximately 40 dB. The measurement of the thin substrate on a quartz wafer, instead of directly placing it on a metal chuck, showed an isolation of about 50 dB. The same flip-chip substrate realized on lossy Si reduced the isolation to about 60 dB.

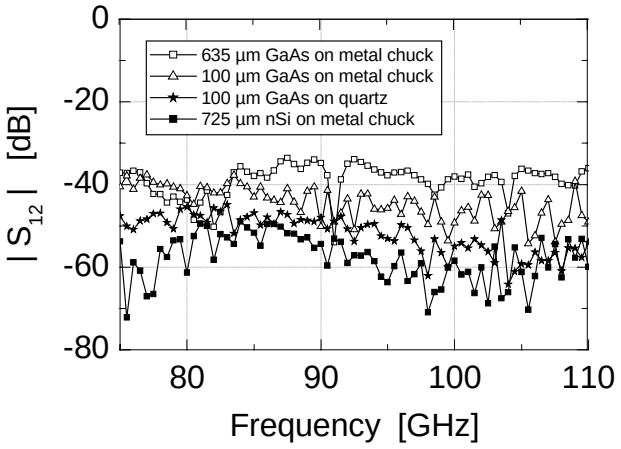

Fig. 6. Measured port-to-port isolation of a flip-chip carrier substrate. The substrate height and material was varied.

V. Flip-Chip Packaging on Lossy Si Substrates

Based on the results obtained in section III and IV, a 94 GHz amplifier MMIC was thinned to 100 µm and flip-chip mounted on lossy n-Si substrates. The Si flip-chip substrates offer not only the advantage of a high suppression of parasitic modes, but also a three times higher thermal conductivity compared to GaAs. The layout of the flip-chip configuration is shown in Fig. 7. FGCPWs and gold bumps were processed on the carrier. For good heat dissipation, the bumps were placed close to the active devices. Other gold bumps were used to realize the RF and DC contacts and to improve the mechanical stability, counteracting the different thermal expansion coefficients of GaAs and Si. The FGCPWs had a center conductor width of 55 µm, a slot width of 32.5 µm, a ground width of 60 µm and a metallization height of 2.7 µm.

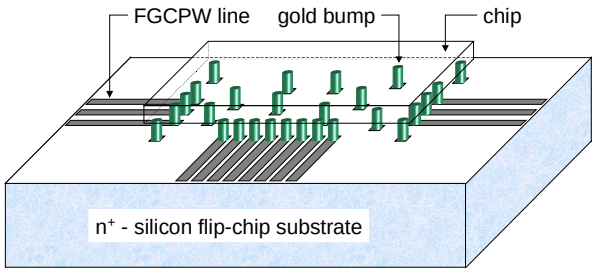

Fig. 7. Layout of a flip-chip carrier substrate with FGCPWs, biaslines and gold bumps.

A comparison between the S-parameters of a thin amplifier chip measured on a quartz wafer and a flip-chip packaged MMIC (100 µm chip on 19 Ω·cm n-Si flip-chip substrate) is shown in Fig. 8. Both measurements showed a very flat gain characteristic from 85 GHz to 100 GHz.

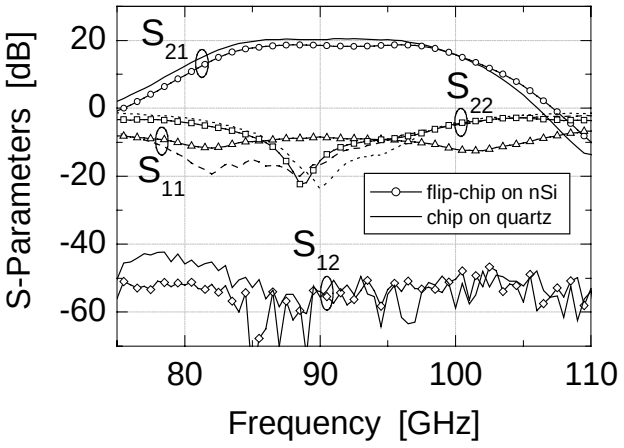

Fig. 8. Comparison between the measured S-parameters of a 100 µm thin amplifier chip on quartz and the same amplifier MMIC flip-chip mounted on lossy Si carrier and measured on metal.

The isolation of both, the amplifier chip on quartz and the flip-chip mounted amplifier was about 50 dB. Because of the additional losses of the doped Si substrate, the small-signal gain of the flip-chip packaged amplifier was slightly reduced by 2 dB. The additional parasitics of the RF bumps caused a small shift for the input and output matching. As shown in Fig. 9, both techniques lead to a µ-factor greater than 1.

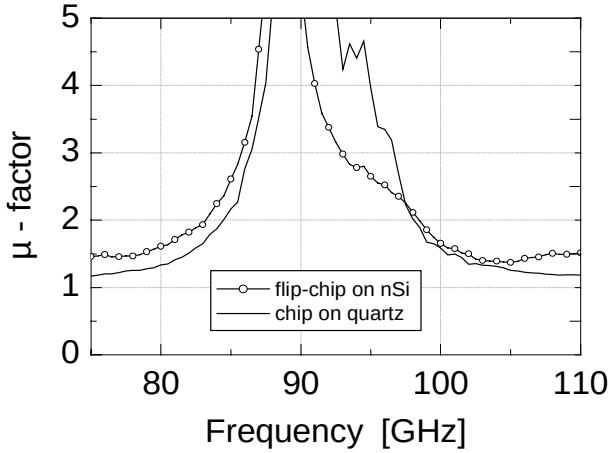

Fig. 9. Comparison between the measured µ-factor of a 100 µm thin amplifier chip on quartz and the same amplifier MMIC flip-chip mounted on lossy Si carrier and measured on metal.

VI. Conclusion

The impact of different mounting configurations for flip-chip packaged coplanar 94 GHz amplifiers was investigated. The excitation of parasitic modes in both, the substrate of the chip and the carrier of flip-chip assembled amplifier MMICs on GaAs mounts, results in circuit degradation or even failure. By thinning the chip and the carrier substrate, the effects of power leakage into substrate modes can be significantly reduced, but only when placing the chips on absorbing material or additional substrates with low dielectric constant, instead of directly on metal. This complicates the fabrication and increases the cost. When flip-chip packaging the thin amplifiers on doped n-Si substrates, we obtain the same results compared to the use of a low dielectric underfill. The lossy n-Si carrier material lead to an efficient suppression of parasitic substrate modes in the carrier chip and thus, to a stable circuit behavior. Aditionally, the Si substrates show a superior thermal conductivity. This makes flip-chip packaging on lossy Si wafers an attractive alternative to conventional GaAs or ceramic substrates.

VII. Acknowledgement

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